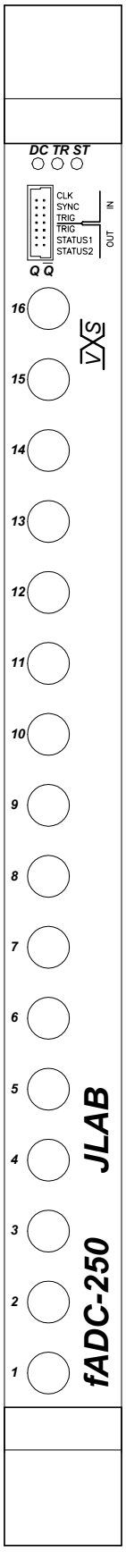

fADC250

VME64x Flash ADC Module Specifications

Signal Inputs	Number	16 S Version (50 Ohm, LEMO)*
	Range	-0.5V, -1V & -2V. User Selectable
	Offset	±10% FS per channel via DACs
Clock	Sampling	250 MSPS, Differential
	Jitter	1 pS (10-bit ADC), 350 fS (12-bit ADC)
	Source	Internal and External
Control Inputs/Outputs	Clock	IN – Diff., LVPECL (Front Panel & Backplane)
	Trigger	IN, OUT - Differential (Front Panel & Backplane)
	Status 1	OUT – Differential (Front Panel & Backplane)
	Status 2	OUT – Differential (Front Panel & Backplane)
	Sync	OUT – Differential (Front Panel & Backplane)
	Trigger SW	Software Strobe (Internal)
Conversion Characteristics	Resolution	10-bit (8 and 12-bit by chip replacement)
	INL	± 0.8 LSB
	DNL	± 0.5 LSB
	SNR	56.8 dB @ 100 MHz Input
	Data Latency	32 nS
Trigger Latency	8 μS	
Data Memory	8 μS	
Data Processing	Sparcification Windowing Charge, Pedestal, Peak Time (Over Threshold, Relative to trigger) Output (Backplane, VXS)	
Interface	VME64x – 2eVME Data Transfer Cycles (40, 80, 160 & 320 MB/sec) with VXS-P0	
Packaging	6U VME64x	
Power	+3.3V, +5V, +12V, -12V	