Hall D -- Trigger "Workshop" 11 March 2008 CCF226

Attendees: Alex Somov; Abhishek Gupta; David Abbott; Fernando Barbosa; Jeff Wilson; Hai Dong; Ed Jastrzembski; Mark Taylor; David Doughty; Chris Cuevas; Elliott Wolin

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Pre-meeting agenda topics are listed below and I have included notes in the summary section for each topic that we covered. Some topics were not discussed, and other topics were discussed as the workshop progressed.

- Agenda Topics

Level 1

FADC250 - Review Trigger Processing Function
(Crate) Energy Sum
Channel organization for BCAL?
Track counting for Tagger,TOF and ?. Any appropriate channel organization issues to discuss?

Global Trigger Crate
SubSystem Processors
Global Trigger Processors
Can we come up with the "Mesh" connection scheme??
More on ATCA.

Fiber Optic Distribution Scheme(Energy Sum & Trigger/Clock)

Trigger Supervisor Crate
Trigger/Clock/Synchronization Distribution
Trigger Supervisor
Clock/Trigger Fanout
Fiber Optic Distribution(Clock/Trigger/Sync)

Review overall timing diagram: i.e. What happens at PRESTART?
Sync-Reset details: How does the multi-crate system starts up synchronously? When do the Crate_Sums start etc?

Propagation delays for each step of the Level 1 trigger. How long does it take to make a decision and how long does it take for Level1 to trigger crates? This must be <<3.5us but it needs to be detailed.

If we have time I would like to talk about a few DAQ topics.
Do we understand the data quantity for each detector section for the expected trigger rates?
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- Summary

We reviewed the simple diagram of the Daq front end crates for the Hall D Trigger and Daq system. The names of the different modules are listed below:

1. **Flash ADC 250** – This is where the Level 1 trigger begins
2. Dave Doughty suggested that the Crate Energy Sum module be named **Crate Trigger Processor**. The reason for the name change is that this module will process Level 1 trigger information from the Tagger crates(Hit Bits), Track Counts from the TOF and Start Counter crates, and the Energy Sum values from the BCAL and FCAL crates. The Hit Bit, Track Count, and Energy Sum processing are embedded firmware functions into each FADC250. The **Crate Trigger Processor** works in concert with the FADC250 modules (up to 16 per crate) to produce an output that is sent to the global trigger crate. The **Crate Trigger Processor** occupies the "A" Switch slot of the VXS front end crate.
3. **Signal Distribution** This module occupies the "B" Switch slot of the VXS front end crates and distributes the required clock, trigger and synchronizing signals to each slot of the front end crate.
4. **Trigger Interface.** This module is specifically designed to reside in physical slot 20(PayloadPort 18) of each VXS front end crate. This module is connected to the trigger supervisor crate via fiber optic cable and provides the interface for the global clock, sync, and trigger signals from the trigger supervisor crate. The **Trigger Interface** module connects directly with the **Signal Distribution** module and provides the control and monitoring of both VXS switch slots.

More discussions followed regarding the **Crate Trigger Processor** and we will need to have a clear diagram that shows the 'trigger processing' capabilities of the FPGA on the FADC250. The three processing functions are listed below:

1. TOF –Tracks
2. Tagger – HITS
3. Energy Sum – BCAL,FCAL

Hai has documented the Energy Sum and initial trigger processing capabilities for the FADC250 prototypes. The prototype units have been tested and CODA library development has started. (Ed and Dave A.)

The next topic of discussion was about specific channel organization from each detector to the FADC250 modules. Alex Somov explained that he is simulating the organization of the channels from the inner and outer BCAL. Results will be presented at another meeting for BCAL and TOF. We had a good example of organizing the TOF counters so that 8 counters(2 PMT/Counter) would fit nicely into one 16 channel FADC250. The track counts could then be processed for the TOF crate using eight counter sections. More simulations are forthcoming.

For the Tagger detectors, the channel assignments are critical and will be organized into the FADC250 on specific channels. These signals are strictly "Hit Bits" and the Crate Trigger Processor(s) will manage these 'Hit Bits' from the fixed hodoscope and moveable microscope devices.

We briefly discussed "window" functions of the Crate Trigger Processor. Should this function happen at the crate level, or at the global level?. I do not have notes that indicate a clear decision, so we should revisit this function (requirement?) soon.

The discussion moved on and Chris showed the details of the entire Level 1 Trigger system for Hall D. These drawings are E size AutoCad files and have been assigned document numbers in preparation for the review. The drawings are divided into two sections for Level 1. The first section shows the connections and fiber distribution scheme for the energy summing. The second section shows the connections and distribution for the clock, sync and trigger signals that will share the same fiber distribution and patch system. Recall that approximately 40 crates participate(create) the Level 1 trigger. The other readout crates in the system are for the CDC and FDC and all crates will need to receive the clock, sync, and trigger signals. The fiber optic cable and patch panel systems have been identified and specified, but we will need to check these specifications before the review.

The remaining drawings show the details of the DAQ readout, Slow Controls, and Terminal Server(ComPorts) network zones that are proposed for the Hall D complex. These network zones originate in the counting house and provide the network infrastructure. and fiber optic trunk cables that will have to be incorporated into the facility installation drawings. We (Mark and Chris) intend to use the information from these 'logical' drawings and create detailed CAD drawings of each instrumentation rack to show the details of all the equipment that is required for the trigger and network systems.

We had a significant discussion on the Global Trigger Crate and I believe I captured the main ideas in the following notes.

The Global Trigger Crate is where the **SubSystem Processor(SSP)** and **Global Trigger Processors(GTP)** reside. The SSP module has been specified in a preliminary document produced by Ben Raydo. The SSP will connect directly to the Crate Trigger Processors. Each SSP is designed to handle up to eight Crate Trigger Processors connections The SSP manage the Crate Trigger Processing data types and feeds this information forward to the GTP. The GTP specification will need to be drafted soon, and the main idea is that each of the SSP modules would connect to multiple GTP in a mesh fabric backplane.

In this method the final global trigger equations could be processed in parallel with each **GTP** managing information from different SSP. It was not determined at the meeting how many **GTP**s would be optimum for the equations necessary for the experiment trigger system. The present design shows, 8 **SSP** (up to 64 Crate Trigger Processors) meshing with 8 **GTP** on a backplane fabric system.

The backplane fabric could be a custom VXS mesh (VITA41.7) or a mesh fabric provided by the ATCA (PICMIG 3.0) standard. There are pros and cons for each selection, with the ATCA solution creating additional work load on limited resources.

As an interim solution, it was mentioned that we could implement the Global Trigger crate using a dual star 'normal' VXS crate. The limitation would be only two GTPs, but we could proceed with design and simulation of the required trigger equations using the latest FPGA processors.

More discussions followed on the best way to connect the final output trigger "word" to the Trigger Supervisor. Assuming that we use an eight GTP solution, only one GTP would connect to the Trigger Supervisor. An 8 bit final output trigger "word" allows for 256 trigger types

The last topic of the workshop was dedicated to the Trigger Supervisor crate and Ed described the modules that are planned for this crate. (I have attached the first page of Ed's document). There are three different modules that are planned for the Trigger Supervisor crate as noted below:

1. **Trigger Supervisor** – VME/VXS payload slot 20 that produces the global clock and trigger signals, plus manages the readout of the front end crate single board computers.
2. **Trigger Fanout** - This is a VXS switch B format that receives the clock, trigger, and sync signals from the Trigger Supervisor and drives these signals to the Trigger Distribution modules.

3. **Trigger Distribution** modules – These are VME/VXS payload modules that receive the signals from the Trigger Fanout switch B module, and connect directly to the front end Trigger Interface modules that reside in each front end readout crate. The connection to each front end Trigger Interface module is via a fiber optic cable.

Workshop adjourned at 4:30pm with no listed action items. Results from trigger simulations will be presented at other Hall D meetings, and the system drawings will continue to be updated.