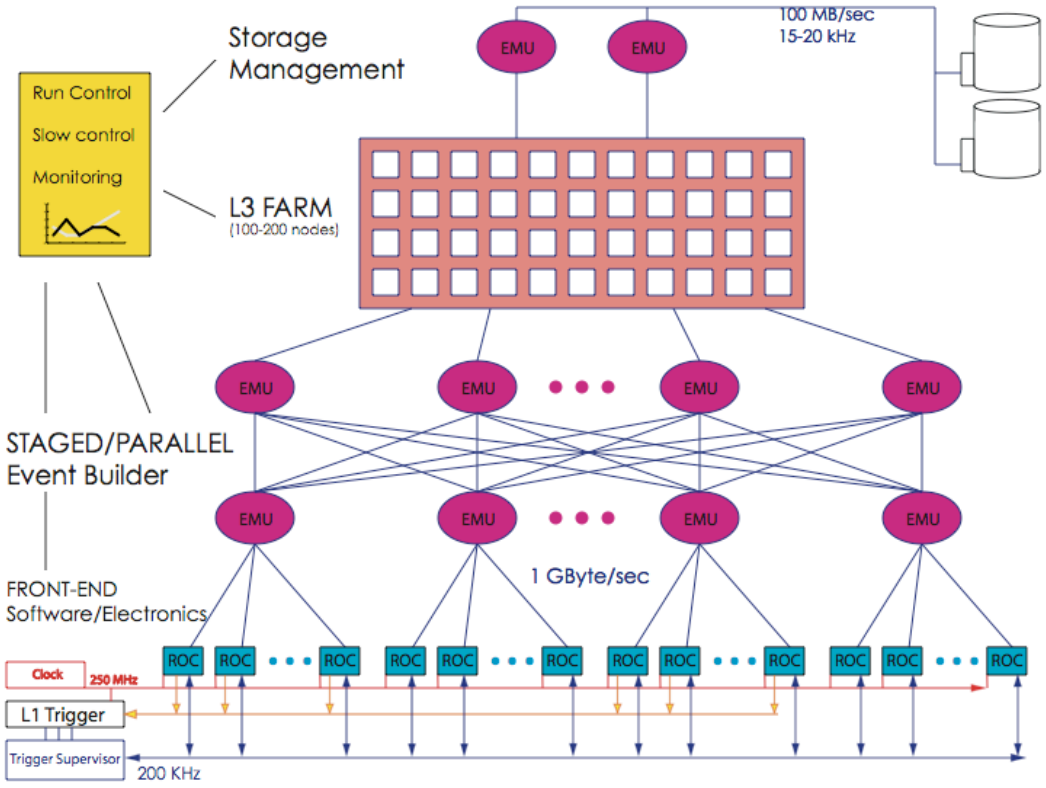
DAQ Update (February 2005)

Gluex DAQ



Requirements:

Pipelined Electronics (ADC, TDC)
- Dead-timeless system
- 200 KHz L1 Trigger

Parallel/Staged Event Building
- Up to 100 Front-end Crates
- 1 GByte/s aggregate data throughput

L3 Online Farm
- 200+ nodes
- x10 reduction in data to disk

GlueX Requirements drive development

Replace aging technologies
- Run Control
- Tcl-Based DAQ components
- mSQL

Maintain cross-platform compatibility (Linux, Solaris, OS X, vxWorks)

Support new commercial hardware advances

Current Active Projects

1. **cMsg** – Homegrown publish/subscribe messaging system which will become the basis for all communication between DAQ Online components. This system effectively replaces functionality currently provided by three separate packages: msql, DP Tcl, and cmlog.
    a. Java-Based with a C/C++ API extension
    b. Lightweight
    c. High performance.
2. **Agent-Based Java Run Control** – Extensible, customizable, with the ability to extend control and monitoring of slow control systems as well as DAQ.
3. **Event Blocking**
    a. Hardware – New VME Trigger interface (Support existing TS)
    b. Software – Parallel readout list for Old ROC
4. **New ROC** – move toward a threaded model for ROC to facilitate multiple CPU front-ends as well as more efficient Linux based versions.
5. **Embedded Linux** – Establish a stable maintainable Linux distribution for single board computers with access to VME and/or PCI hardware.
6. **Flash ADC** – Development of pipelined ADC for deadtimeless front-end digitization including triggering support.

Near term projects

1. **ET-Based Event Builder/Data Concentrator** – EMU Necessary for support of staged parallel Event Building from many sources (ROCs)
2. **Large-scale development/testing DAQ farm –** currently the only large test bed for understanding complex DAQ systems is the CLAS detector. Availability of this system is limited.

Longer-term projects

1. **Online farm** – Support for L3 trigger and event filtering/analysis
2. **New Trigger Supervisor/High Speed Clock Distribution**