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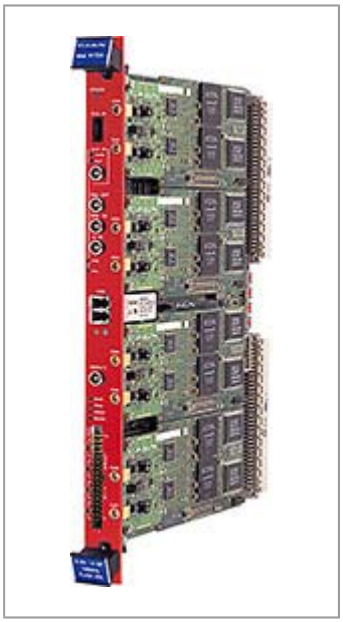
Nuclear Physics

**Family: VME**
**Model: V1724**

**V1724 - 8 Channel 14 bit 100 MS/s Digitizer**

**New**



## Highlights

- **8 channel**
- **External Trigger or programmable voltage threshold for automatic triggering**
- **14 bit 100 MS/s ADC**
- **Front panel clock In/Out available for multi-board synchronisation**
- **External ADC clock input or PLL synthesis from internal/external reference**
- **Lower and variable frequency sampling available**
- **Trigger Time stamps**
- **512 ksamples memory per channel (expandable)**
- **Programmable event size and prepost trigger adjustment**
- **VME64X compliant interface**
- **Optical Link interface**
- **A2818 PCI controller available for handling up to 8 V1724 daisy chained via Optical Link**
- **FPGA firmware upgradable via VME**
- **Demo software tool for board control with CAEN VME bridges (V1718,V2718, VX1718, VX2718)**

## Overview

The Mod. V1724 is a 1-unit wide VME 6U module housing a 8 Channel 14 bit 100 MS/s Flash ADC Waveform Digitizer with threshold Auto-Trigger capabilities.
The single ended analog input signal has a dynamic range of ±1.125 V or ±5 V.
The DC offset of the signal can be adjusted channel per channel by means of a programmable 16bit DAC.
The board features a front panel clock/reference In/Out and a PLL for clock synthesis from internal/external references. This allows multi board phase synchronizations to an external standard or to a V1724 clock master board.
The data stream is continuously written in a circular memory buffer; when the trigger occurs the FPGA writes further N samples for the post trigger and freezes the buffer that then can be read either via VME or via Optical Link; the acquisition can continue without dead-time in a new buffer. Each channel has 512 ksamples (expandable up to 2 Msamples and over) of SRAM memory, divided in buffers of programmable size from 500 sample x 1024 buffers (5 µs window) to 256 ksamples x 2 buffers (2.56 ms window).
The trigger signal can be provided via the front panel input as well as via the VMEbus, but it can also be generated internally, as soon as a programmable voltage threshold is reached. The individual Auto-Trigger of one channel can be propagated to the other channels and onto the front panel Trigger Output.
The VME interface is VME64X compliant and the data readout can be performed in Single Data Transfer (D32), 32/64 bit Block Transfer (BLT/MBLT) and Chained Block Transfer (CBLT).
The board houses a daisy chainable Optical Link able to transfer data at 125 MB/s, thus it is possible to connect up to eight V1724 (64 ADC channels) to a single Optical Link Controller (Mod. A2818, see Accessories/Controller).

The V1724 can be controlled and readout through the Optical Link in parallel to the VME interface.

| Technical Specifications Table | |
|---|---|
| **Package** | 1-unit wide VME 6U module |
| **Analog Input** | 8 channels, 50MHz Bandwidth, 2V or 0.5V input range, positive or negative, programmable DAC for Offset Adjust single-ended (MCX - 50Ohm) or differential (Tyco 3 pin - 100Ohm) |
| **Resolution** | 14 bit |
| **Sampling Clock** | External Clock Input (LVDS, NIM, TTL) and Output (TTL, NIM). Internal 20MHz quartz.<br>Direct ADC feed or clock synthesis with low jitter programmable PLL<br>Multi board synchronization (one board can act as clock master)<br>External Clock Gate (NIM or TTL) for burst or single sampling mode |
| **Memory** | 512 KB/ch expandable up to 8MB/ch, Multi Event Buffer with independent read and write access<br>Programmable event size and pre-post trigger. Up to 2048 events.<br>64 Ksample max record lenght (corresponding to 640us digitization) |
| **Trigger** | Common External TRG-IN (NIM or TTL) and VME Command<br>Individual channel autotrigger (time over/under threshold, energy trigger or other programmable logic)<br>TRG-OUT (NIM or TTL) for the trigger propagation to other V1724 boards<br>32 bit Trigger Time Stamp. Sync Signal to synchronize the internal time counter to an external reference |
| **Trigger Time Stamp** | 32bit – 10ns (43s range)<br>Sync input for Time Stamp logging |
| **FPGA signal process** | One Cyclone EP1C4 or EP1C20 per channel<br>Fully programmable digital filters (Deconvolution Moving Window, Trapezoidal FIR Filter, Pole-Zero Cancellation, Energy and Time extraction)<br>Firmware downloadable via VME by the user |
| **Optical Link** | Data readout and slow control with transer rate up to 125MB/s<br>Daisy chainable: one A2818 PCI card can control and read eight V1724 boards in a chain |
| **VME interface** | VME64X compliant<br>D32, BLT32, MBLT64, CBLT32/64 and Multi Cast Cycles<br>Transfer rate: 60MB/s<br>Sequential and random access to the data of the Multi Event Buffer<br>The Chained readout allows to read one event from all the channels in a VME crate with a BLT access |
| **Upgrade** | All FPGAs firmware can be downloaded from VME |
| **Software** | General purpose C and LabView Libraries and Demo Programs |
| **Analog Monitor** | 12bit / 100MHz DAC output able to reproduce the waveform at the different stages of the filters<br>Majority current sum (1mA per triggered channel, chainable between boards) |
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| **LVDS I/O** | 16 general purpose LVDS I/O controlled by the FPGA<br>Busy, Data Ready, Memoru full, Individual Trig-Out and other function can be programmed<br>An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker |

| **Ordering Options** | |
|---|---|
| **Code** | **Description** |
| **WV1724XAAAAA** | V1724 - 8 Ch. 14 bit 100 MS/s Digitizer |