Contents

Chapter 7

Readout Electronics

7.1 Overview

The goal of the HALL Dreadout electronics system is to digitize the detector signals without incurring deadtime. Two basic types of readout electronics will be used in HALL D, FADCs and TDCs. Detectors which measure energy will be continuously sampled with flash ADCs while detectors which require precise time measurements will use a multi-hit TDC. The digitized information must be stored for several μs while the level 1 trigger is formed. No currently available commercial solutions exist. These boards would be designed by our collaboration.

7.2 Calorimeter FADCs

The calorimeters will be read out with 8-bit linear FADCs. A single channel prototype of the calorimeter FADC has been designed and built at Indiana University. A block diagram is shown in Fig. 7.1 and a photo in Fig. 7.2.

A differential amplifier inverts the negative PMT signal and shifts the voltage levels to match the input range of the digitizer integrated circuit. The digitization is performed by an SPT7721 manufactured by Signal Processing Technologies [1]. This IC costs about US$25 each in small quantities. An 8-bit value is produced every 4 ns; two samples are output every 8 ns or 16 bits at 125 MHz.

All digital functions are performed in a Xilinx [2] XC2S50 programmable gate array. This IC costs about US$15 each in small quantities. A dual port RAM configured as a circular buffer stores the data for 8 microseconds. Upon receipt of a trigger signal the data from the time window of interest is copied

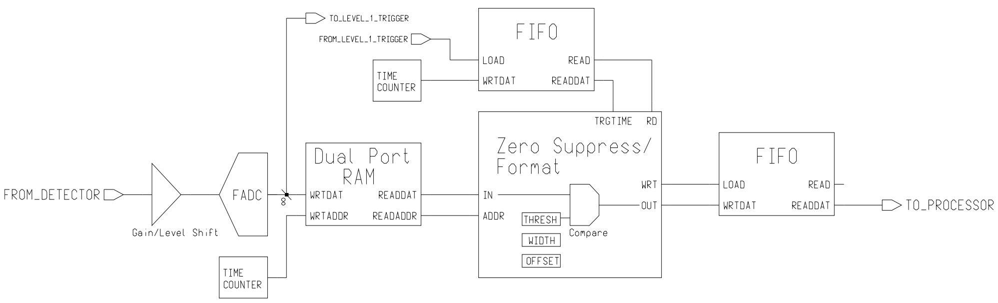

Figure 7.1: Block diagram of prototype FADC board.

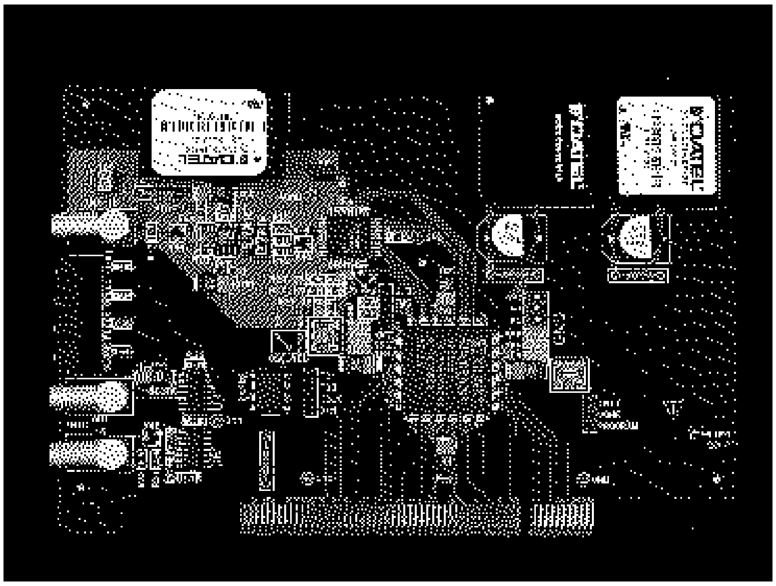

Figure 7.2: Photograph of prototype FADC board.

to an output FIFO. This FIFO is interfaced to a 32 bit, 33 *MHz* PCI bus. More information on this prototype is available [3].

The final version of the calorimeter FADC will include adders which continuosly sum the digitized information from all channels. This energy sum will be used in the level 1 trigger.

7.3 Tracking FADCs

The Central Tracking Drift Chamber will be readout with 8-bit nonlinear FADCs. The digitizer will be preceded by a logarithmic amplifier which will compress a 10-bit dynamic range down to 8 bits. The anode FADCs will accept negative going signals, while the cathode FADCs will accept positive going signals.

7.4 TDCs

The Photon Tagger, Forward Drift Chambers, Start Counter, Barrel Calorimeter, and Time of Flight Wall will be read out by multi-hit TDCs. Such a high resolution pipeline TDC module has been developed for use at Jefferson Lab, and is designed to meet the requirements of current experiments, as well as to serve as a prototype for future experiments, including Hall D. The design is implemented as a VME-64x module. This bus standard was chosen because it is already in use at Jefferson Lab, has good (and evolving) data transfer capabilities, and reasonable channel densities are possible.

The module is built around the TDC-F1 integrated circuit from Acam-Messelectronic Gmbh [4]. The TDC-F1 chip was designed for the COMPASS experiment at CERN [5]. It includes many features that will be useful in experiments at Jefferson Lab. This chip utilizes purely digital delay techniques to measure time. In normal mode the TDC-F1 chip provides 8 input channels with up to 120 ps resolution (LSB). In high resolution mode channels are combined in pairs to yield up to 60 ps resolution for 4 input channels. The dynamic range for measurement is 16 bits. The resolution of the chip is tunable about its nominal value. A PLL circuit adjusts the core voltage of the chip to compensate for temperature and supply voltage variation, assuring stability of the resolution value. On-chip buffering for input channels, triggers, and output data allows for multihit operation with nearly zero deadtime. The chip also has a complex trigger matching unit that can filter out hits unrelated to the input trigger. When enabled, only hits that are within a programmed timing window relative to the trigger time are kept.

The 8 TDC-F1 chips on our module provide 64 channels in normal mode, or 32 channels in high resolution mode. A 128K word deep FIFO is attached to each TDC-F1 chip to buffer its output data. The module can be set up to interrupt the crate controller after a programmable number of triggers have been received. During read out the module will provide a block of data associated with a programmed number of triggers, and then terminate the transaction.

To enhance system performance a set of TDC modules may be read out as a single logical read using a multiblock read protocol. This involves passing a token between modules along a VMEbus daisy-chain line. In this setup, only the first module in the chain will generate the interrupt, and only the last module in the chain will terminate the transaction.

The TDC module is fabricated as a single 12-layer printed circuit board. Six of these layers carry signals on 5 mil wide traces. Internal layers are organized in a stripline configuration and have a characteristic impedance of 50 ohms. High-speed ECL components are used for the front end. Logic in a single FPGA chip (484-pin BGA) controls the entire module. The high density of the design demands that surface mount components be installed on the front and back sides of the board.

7.5 High Voltage

The Forward Calorimeter PMTs will be powered by Cockcroft-Walton voltage multipliers [6]. This type of base provides for very low power consumption and is controlled over a serial communication link. The Barrel Calorimeter hybrid PMTs, Cerenkov PMTs and Time of Flight PMTs may be powered by similar circuitry. The Tracking Chambers will probably be powered by a commercial HV power supply with sensitive current monitoring.

7.6 Packaging

The FADC circuit requires about 50 cm^2 of board space and adjacent channels will need to be about 2 - 3 cm apart. This implies a density of about 8 channels on a 6U board or possibly 16 channels on a 9U board.

Assuming 8 channels on a 6U board with 20 boards per crate and 5 crates per rack yields 800 FADC channels in a rack. The 2200 Forward Calorimeter channels will then require 3 racks. The 576 Barrel Calorimeter channels will occupy one rack. The 5200 Central Drift Chamber Anode FADCs will need 7 racks and the 5760 Forward Drift Chamber Cathodes will need 8 racks.

In the low resolution (120 ps) version of the TDC 64 channels fit on a 6U board. This version of the TDC is used for the 2880 Forward Drift Chamber anodes and the 2000 Start Counter Fibers. At 1280 channels per crate, 4 crates or 1 rack are required.

The Photon Tagger, Start Counter Scintillators, Barrel Calorimeter, and Time of Flight Wall require the high resolution (60 ps) version of the TDC.

640 channels fit in a crate, so the 1200 channels in these detectors will occupy 2 crates.

7.7 Readout Bus

FASTBUS crates are no longer being manufactured, and are not being considered for HALL D. CAMAC crates are fairly slow and have limited board space and power available. Some legacy devices may be packaged in CAMAC, but not the bulk of the readout electronics.

VME is popular at Jefferson Lab and the TDC prototype is constructed on a VME64x card. Compact PCI is used extensively in the telecommunications industry and can be driven directly by typical FPGA ICs without the need for bus interface ICs. Predefined PCI interface "cores" are available, minimizing design time. One disadvantage of cPCI is that bridges are required for a system with more than 8 slots, although there are commercial bridges available.

VXI and PXI are "instrumentation" extensions to VME and cPCI. Shielding, triggering, clock distribution, and additional power are added to the basic bus standard.

The FADCs require low skew fanout of the 250 MHz clock. The need to form a digital global energy sum for the level 1 trigger will probably drive the choice of packaging for the calorimeter FADCs. Some sort of custom backplane will be required to support the tree of adders.

The telecommunications industry is moving towards "Switched Serial Fabrics." This adds a high speed serial connector to the backplane which can support Ethernet and other high speed serial technologies. For VME the applicable standard is VXS (VITA 41) and for cPCI the standard is PICMIG 2.16. For a 16 channel FADC module producing 25 bytes per channel per level 1 trigger; a level 1 trigger rate of 200 kHz; and a 2% occupancy the data readout bandwidth required for a module is 16 Megabits per second, well within the capability of a 100baseT Ethernet connection.

7.8 Construction

7.9 Manpower

List of Figures

List of Tables

Bibliography

[1] Signal Processing Technologies:
`http://www.spt.com`.

[2] Xilinx:
`http://www.xilinx.com`.

[3] More information on the FADC prototype can be found at
`http://dustbunny.physics.indiana.edu/~paul/hallDrd`.

[4] Details of the "F1" chip can be found at
`http://www.acam.de`.

[5] COMPASS experiment at CERN:
`http://wwwcompass.cern.ch`.

[6] A. Brunner *et al.* A Cockcroft-Walton base for the FEU84-3 photomultiplier tube. *Nuclear Inst. and Meth.*, **A414**:466, 1998.