# Some Agenda Items & Points for Discussion for GV visit (1/29 – 2/1) to JLab for GlueX FDC

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## *Labwork with FDC prototype*

The principal purpose of the visit is to work with Simon to:

1. Ensure that the new receiver/shaper boards are optimally incorporated into the FDC prototype setup, and decide on any design tweaks that may be called for
2. Check for any spurious signals, feedback, reflections, noise issues, etc., and attempt to address them
3. Check/confirm the signal level / gain of the detector, I would probably like to do a direct comparison to a step voltage pulse capacitively coupled to preamp while it is still connected to detector.
4. Measure the cathode strip capacitance per unit length (I haven't seen mention of any measurement of this yet…?)
5. Measure the noise spectrum with preamp on the detector, first through the VPI post-amp box and second through the receiver/shaper board
6. Check/improve feed of timing stop signal to ADC's
7. Set up external clock source to ADC's from synthesizer (Chris states he can find one for medium-term loan for this purpose). [We'll need a NIM leading-edge discriminator too, I'd guess you have one. We'll also need simple software changes to allow external clock usage (hopefully switchable).] Purpose is:
    a. Make timing measurements across boardss, e.g. anodes & cathodes
    b. Provide flexibility in frequency, which is absolutely critical to any serious attempt to experimentally decide what sample frequency is required for the new ADC board (which is in turn absolutely critical to designing or even costing the new ADC board, which is due soon)
8. Look at signals, discuss & explore timing algorithm & results, decide if changes to peaking time are needed (I will bring parts for at least one longer shaping time to patch onto a few channels in case it is warranted)

## *Handoff of parts & documentation for receiver/shaper board stuffing*

I will bring all required parts and bare boards necessary to build up an additional 6 receiver/shaper boards. The work will be completed by a technician supervised by Chris. At least one more board should be completed as soon as possible and sent to CMU for use with the CDC prototype setup. The remaining 5 should probably be built up completely *except* for the shaper components (one resistor, two capacitors, two inductors per channel), pending the outcome of timing tests. It is conceivable that the optimum peaking time should be increased or decreased from the present ≈23 ns.

## *Signal cable and connector discussions*

It is not clear to me at this time that we are all in agreement about the signal cables and connectors, or that, if we are in agreement, that we have been consistent everywhere. Certainly the FDC budget justification document shows a different type of cable (though it doesn't specify a real part number) than Fernando and I have been assuming. I think there are several semi-independent issues:

1. Number of conductors (and hence number of channels per cable). I think both Fernando and I have stated 24 channels (50C). I think Fernando intends this _even_ in case of F1TDC readout of anodes. Maybe I understand that wrong. How will that be connected at the F1TDC end, which is a 64-ch board? I do very much still prefer 24 channels per cable and a 72-channel ADC board. Besides the channel count of the ADC board, advantages for the 24ch option are in the reduced cable count and cable cross-sectional area.
2. We all agree (I'm sure) that the cables will be mass-terminated, i.e., IDC connectors. We also all agree (I'm sure) that the cables will have an overall shield, and will consist of twisted pairs.
3. Pitch of the IDC (flat sections) – can be either 0.025", 1mm, or 0.050". But 1mm is probably not available with the other characteristics we need, anyway I don't know of it. So the choice is half-pitch 0.025" or the standard 0.050". The advantage of the former is that both the connectors and the cable are smaller and lighter. There are also more styles of connectors available, including connectors with a protective backshell that would be desireable at the ADC board end. The advantage of the latter is that everybody's used it before, and it is slightly cheaper. Signal quality is similar, both will suffer serious frequency-dependent signal loss in 100 foot length, that must be compensated (by the design of the preamp or the ADC board or both). [For discriminator output compensation is not required unless the rate is very high, only for the analog signal transmission.]
4. Safety requirements. I don't see how anyone can possibly cost the cables unless the safety requirements are specified. I asked Chris yesterday, what type of cable is required, specifically is halogen-free cable required? Answer was, he didn't know yet but was expecting to learn this soon. Anyway, I have been holding off getting a real quote or estimate on the 0.025" cable because I couldn't answer to the vendor what the requirements were.
5. Who will assemble the cables? That may have some impact on the decision, for instance some types of 0.025" cable connectors may not be suitable for hand assembly by young grad students…
6. In the end, all *I* need is to know what connectors go on the ADC board. So, if it is thought that I shouldn't worry about 1-5 above, I can accept that; just specify the connector and I'll go with it.
7. Cable loss does need to be compensated (equalized) over frequency. This is best done on the ADC board, because of preamp voltage compliance limits and because the exact cable length and attenuation can be decided later (just prior to stuffing of all the production ADC boards).

## *Preamp ASIC & Board Discussions*

I think there are two main issues to discuss, and then a couple of other details:

1. Signal termination scheme. Objectives are:
    a. Transmit the signals without reflection (<1%)
    b. Keep voltage at ASIC terminals (and everywhere else too, of course) within linear region
    c. Deal with realistic ground voltage differences between preamp board and ADC boards.
    d. Prevent (ok I mean reduce) common mode currents, that would (presumably inevitably) couple through the ground pins that connect preamp board to the chamber planes. I think that the proper way to address this is by providing a high common-mode impedance either at the preamp end or at the ADC end of the cable. Since the ASIC has such a narrow voltage compliance, given point c above I think it is required to provide a high common-mode impedance at the ADC board, with a reasonable compliance range (a couple of volts).
    e. Yes this does (I think) imply double-termination, but that's good for point a above, and anyway it does not imply a significantly higher noise. For example, this is what is now implemented with the CLAS preamps and the receiver/shaper board, and the noise is completed dominated by the preamps still. (But yes, the new ASIC is expected to be less noisy.)
    f. Preamp board should be laid out to allow termination, and with cuttable common-mode termination, so we can test it.
2. What to do with the last pair in the cable (either the 25 pair or the 17 pair cable has one)?
    a. I think the ADC board should drive it as an LVDS signal to the preamp board, to control an on-board pulser and any other control parameters. In case of TDC readout, a revised F1TDC board could do same, and this mechanism can program the thresholds as well as provide test pulse.
    b. If so, some kind of pulse-width encoding would be used, in conjunction with very simple timing discrimination on the preamp board, e.g. with R-C timing circuits. Probably three pulse widths are needed, one for "start" or "strobe", one for a serial bit 1, one for a serial bit 0. The data rate would be fairly limited (for example, new pulser amplitude would take few tens of ms) but I'd think that's ok.
    c. If we defined a (reasoanble) scheme, it could be incorporated into the ASIC in a next version, so no (or few) extra components needed on preamp board for this.
    d. If a-c above are voted down, of course we can just use the pair to send analog pulser signal. I'd favor though to drive it differentially, and receive it with a balanced termination, and preferable actually use the difference voltage as the pulser signal. Transformers are not an option in the magnet, but a simple pair of transistors might convert it to single-ended, or else better maybe we just apply it differentially to the ASIC since it has a differential input anyway.
    e. In case of d, then any needed control has to come through the power distribution system, ok I guess.

3. As a minor point, I'd suggest use SDA004 for the protection diodes, very small but rugged
4. We should note that Mitch at least orginally recommended[1] an intermediate signal repeater board located probably just outside the magnet. I do not like the idea of the signal repeater board, it is a lot of extra connectors, power supplies, place to mount boards is needed, etc. It's also not in the current baseline plan, right? I think with careful handling of the termination and a good clean system ground plan, there should be no need for the signal repeater board. But, we should probably discuss.
5. Cathode/anode gain selection would ideally be done in the preamp ASIC, like a pin strap to select one of two gains. Doing it at the ADC board end is possible, but will result in higher noise level on the cathodes than if this is handled in the preamp ASIC. I don't remember what our current plan is...?

## *ADC board issues*

It is early for me to be able to ask the questions, since I haven't begun to work on the back end of the ADC board at all, but if there is any time left beyond the other items, it would be good to find out details (especially what is now being done for fast ADC board, and for F1TDC board) for:

1. Data formatting – I assume all data for a given event should wind up contiguous in memory, followed by data for later events. And that within an event, all data for a given channel (passing zero suppression) is contiguous, followed by next channel. This is contrary to Struck ADC scheme. Note event data is variable size, even if number of samples per channel is fixed.
2. Channels are zero suppressed if waveform _never_ is over threshold during the predetermined sample range (N ticks before trigger, M ticks after) ?? Or supressed if only one particular predefined sample point is not over threshold??
3. How many events shall buffers be sized for? (Or else, how many kBytes per channel actually being designed in fast ADC board today?) This was answered before but...

## *FDC Detector*

I'd just like to see/understand the design details, for instance how the preamp boards connect, what is the bias & AC coupling scheme. I saw some docs posted about it, looks good overall I think. I have a concern about signal coupling through the field wires (maybe some bypass cap should be added).

## *Project Issues*

Assuming it is mutually agreeable, I'd propose to keep working on this over the coming year as previously planned. The principal objective would be the development of a prototype 72-channel ADC board. We need to discuss extension of time for the present contract and need to get going to set up a succeeding contract.

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[1] For same reasons, I think, as my worries in point 1 above.